AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (currently amended) A probe card for testing a semiconductor chip, comprising:

a plurality of probes;

a build-up interconnection layer having a multilayer interconnection structure therein, said interconnection structure comprising plural interconnection layers and one or more resin insulation layers insulating said interconnection layers from each other, said build-up interconnection layer carrying said plurality of probes on a top surface thereof in electrical connection with said multilayer interconnection structure; and

a decoupling capacitor embedded entirely within and completely covered on its top surface by said resin insulation layer constituting said build-up interconnection layer in electrical connection with one of said probes via said multilayer interconnection structure,

said multilayer interconnection structure including an inner via-contact in the vicinity of said probe.

Claim 2 (original) A probe card as claimed in claim 1, wherein said capacitor has a thickness generally equal to or less than a thickness of said resin insulation layer.

Claim 3 (canceled).

Claim 4 (currently amended) A probe card as claimed in claim 1, wherein said capacitor is formed in said build-up interconnection layer~~, right~~ directly underneath one of said probes.

Claim 5 (canceled).

Claim 6 (original) A probe card as claimed in claim 1, wherein said capacitor includes a dielectric film of a complex oxide containing at least one metal element selected from the group consisting of Sr, Ba, Pb, Zr, Bi, Ta, Ti, Mg and Nb.

Claim 7 (previously presented) A probe card as claimed in claim 1, wherein said capacitor includes upper and lower electrodes sandwiching a dielectric film, said upper and lower electrodes containing at least one metal element or a metal oxide selected from the group consisting of Pt, Au, Cu, Pb, Ru, a Ru oxide, Ir, an Ir oxide, and Cr.

Claims 8-9 (canceled).

Claim 10 (original) A testing method of a semiconductor device by using a probe card, said probe card comprising: a plurality of probes; a build-up interconnection layer having

a multilayer interconnection structure therein, said build-up interconnection layer carrying said plurality of probes on a top surface thereof in electrical connection with said multilayer interconnection structure; and a capacitor embedded in a resin insulation layer constituting said build-up interconnection layer in electrical connection with one of said probes via said multilayer interconnection structure, said multilayer interconnection structure including an inner via-contact in the vicinity of said probe,

said method comprising the steps of:

causing said probe card to make a contact with a semiconductor chip to be tested such that said semiconductor chip is in electrical connection with said probe card; and

testing electric properties of said semiconductor chip,

said method further comprising the step, before contacting said probe card to said semiconductor chip, of setting an impedance between said probe and said capacitor to be substantially equal to an impedance of a semiconductor package including therein said semiconductor chip and a capacitor, for a part between said semiconductor chip and said capacitor.

Claim 11 (original) A testing method as claimed in claim 10, wherein said test is conducted in the state said semiconductor chip forms a semiconductor wafer.

Claims 12-31 (canceled).